

Part No: 10281

Functions

- Controlled by up to 5 ref. frequencies
- Phase coherent fail-over
- Averaging of the ref. frequencies.
- Facility for constant, linear and for quadratic offset control
- Very low phase noise BVA oscillator as internal frequency source
- Clock ensembling improves the longterm frequency stability
- On-line monitor of the input stability
- Monitor data stored for postprocessing in an external PC
- File format compatible to STABLE32

Inputs

Standard: all 100 MHz Configuration:

100 MHz 5 ports

Option: with 5 / 10 MHz Configuration:

100 MHz 4 ports 5 / 10 MHz 1 port

Outputs

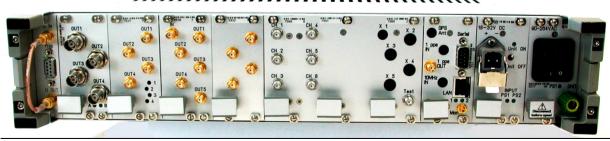
Standard: 7 outputs

100 MHz 3 ports 5 MHz 4 ports

Option: 11 outputs

100 MHz 7 ports 5 MHz 4 ports





The unit shown on the photo is equipped with SW download interface in slot #0, with the option 4 (high performance 5 MHz output) in slot #2 and with a test output module in the slots #3. The SW download interface and the test output module are not part of the product itself.

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

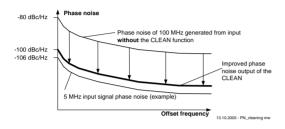
Part No: 10281



Clean-up Oscillator front panel label and acronym in text: CLEAN

Clean-up Oscillator Applications

I Phase noise clean-up with 100 MHz generation

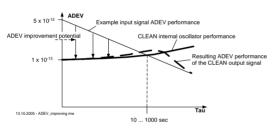


Phase noise over offset frequency, improvement by internal oscillator performance

The output frequency of commercial atomic clock equipment (e.g. Rubidium, Caesium, Hydrogen maser) is at 5 MHz, 10 MHz, or 100 MHz. Its phase noise is good, but it can even be improved by the CLEAN. Especially when generating 100 MHz clock reference signals (e. g. for reference input to up-converters) an excellent phase noise performance is essential because improving the phase noise of the reference signal directly improves the signal to noise ratio of the generated RF signal.

The CLEAN generates a very low phase noise output at 100 MHz.

II Improving the ADEV stability

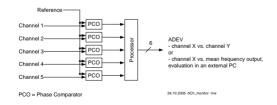


Short term ADEV over tau, improvement by internal oscillator performance

The output frequency stability of commercial atomic clock equipment is very high in the long term, but in the short term further improvement is possible. The internal oscillator of the CLEAN provides enough short term stability for significantly improving the stability of a Cesium reference clock. This improves any time interval measurements up to time intervals of several 100 seconds. As the improvement is achieved by the internal oscillator intrinsic phase stability performance the improvement factor depends on the stability of the

reference input. Less stable input leads to a higher improvement factor. The time constant of the internal oscillator control loop can be adjusted for optimising the performance.

III Clock ensemble monitoring



Phase measurement of 5 input channels, ADEV output for 6 channel combinations

The outputs of a set of atomic clock equipment can be monitored against each other by means of a 5 channel phase comparator function of the CLEAN.

The 5 phase comparators measure the phases of 5 input signals versus a reference clock signal. The processor allows calculation of ADEV performance of any channel versus any other channel or of any channel versus the reference input. Normally the reference is the internal oscillator output, but the

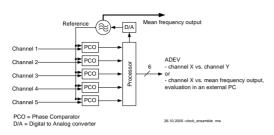
equipment allows for using an external reference as well (if controlling the internal oscillator is not required).

 $5\,/\,10\,/\,100$ MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

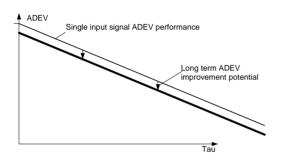
Part No: 10281



IV Real time averaging of reference clocks



Controlling the internal oscillator to the mean frequency of up to 5 input channels.



26.10.2005 - Clock_ensemb

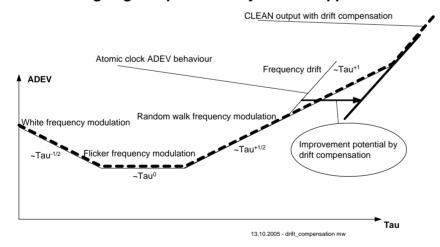
Based on the monitoring function as described above the CLEAN can generate the mean frequency and phase of a clock ensemble in real time. The reference clock for the phase measurements is the CLEAN output signal.

The averaging of the measured phase and frequency data for controlling the internal oscillator is done by the internal processor. The frequency generation function of the CLEAN is independent of the availability of any external computer.

In the best case of 5 inputs of equal ADEV performance the improvement factor is SQRT(5) = 2.2.

ADEV improvement by clock ensembling

V Clock ageing compensation by micro-stepper function



Long term ADEV over tau, improvement by drift compensation

The CLEAN implements a micro stepper function. This allows for adding an arbitrary correction signal to the internal oscillator control signal. The clock model within the processor supports generating a phase offset, a frequency offset, and a frequency drift offset. These offsets can be generated for compensating corresponding offsets of the input channels individually for each channel.

While the phase offset and the stationary frequency offset do not contribute to the ADEV the frequency drift offset does.

Therefore, compensating this drift offset improves the ADEV of the CLEAN output in the long term.

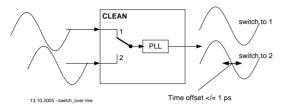
The drift value to be compensated can be measured by comparing the relevant input channel against the UTC (e. g. applying two-way time transfer from a suitable reference source) or, in case of a clock ensemble with non equally performing clocks, any worse performing input clock signal can be compared to the CLEAN output signal as the most stable reference of the site.

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



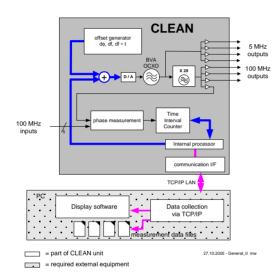
Phase continuous switch over between several input sources



When the CLEAN is tracking a single selected input channel it can switch over to another input channel. Such switch over is phase continuous with a residual phase error of one picosecond or less.

Switch over with resulting time offset less than one pico-second.

Clean-up Oscillator Functions



The CLEAN System consists of three parts

1. CLEAN Hardware.

Internal Oscillator.

A combination of an ultra stable BVA OCXO 5 MHz and the low phase noise 100 MHz VCXO generates high purity 5 MHz and 100 MHz output signals.

Phase Comparator.

The 5 input channels are measured against the internal reference signal being provided by the internal oscillator. The phase offset results of these measurements are provided to the internal processor.

Phase Locked Loop.

The internal processor can control the internal oscillator by setting the oscillator control voltage. When deriving the control data from a single input channel phase

measurement data then an ordinary PLL is realized. However, it is also possible to derive the oscillator control from several input channels calculating mean values. In addition to the pure control by input signals the CLEAN allows for adding a programmed offset signal to the oscillator control voltage. The offset signal is generated by the offset generator.

Offset Generator.

The offset generator can generate offset values for

- Constant **phase offset** with 10⁻¹⁵ seconds resolution.

 Constant **frequency offset** with 10⁻¹⁸ fractional frequency offset resolution.
- Constant frequency **drift offset** with 10⁻²¹/s fractional frequency offset per second resolution.

2. Embedded Monitor & Control Software

This S/W is used to control the functions of the CLEAN, monitor the integrity of its H/W functions and configure the input frequency of the frequency multipliers. This software is part of the CLEAN unit and runs on the embedded processor inside this unit. It allows fully stand-alone operation of the unit.

3. External Display Software

This S/W additionally provides a graphical visibility of what is going on inside the CLEAN. It shows the phase and frequency evolution and performance including ADEV calculation of all input signals, selected combination of input signals and gives a real time performance assessment of the CLEAN output. This software requires an external PC.

The data is collected in files the format of which is compliant to the needs of the STABLE32 software. Storage capacity of an external PC is required for this.

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



Clean-up Oscillator Modular Architecture

Modular unit design

The Clean-up Oscillator is a two height unit rack mountable unit consisting of up to 10 modules. The optional modules can be hot plugged without impacting the operation of the unit. Dedicated slots are carrying the essential modules such as the AC/DC Converter, the DC Supply Module, the PC Module and the Oscillator Module. All modules are mounted from the rear side. All signal inputs and outputs are also at the rear side.

The CLEAN frame

At its front panel the instrument has a LCD display and 8 push buttons for local control of the unit. LEDs on the front side show the over all alarm state (ERROR) of the unit, the DC power supply integrity and the remote control disabling (LOCAL).

Modules providing the input ports

The 5 external inputs at 100 MHz are at the PCO module This module is an assembly occupying three slots of the CLEAN frame.

With the option #2 one input at 5 or 10 MHz is made available by adding a multiplier module. The output of this module is connected to an input channel of the PCO by an external patch cable.

Modules providing the output ports

The CLEAN product has the following output signal types

- Multiplier module: 100 MHz, 4 outputs. One of these 4 outputs is needed for reference input to the phase comparator module, 3 of the outputs are usable externally.
- Oscillator module: 5 MHz, 4 outputs at BNC connectors for standard performance applications
- 100 MHz distributor module: 4 outputs at SMA connectors for high performance applications (option 1)
- 5 MHz distributor module:, 4 outputs at SMA connectors for high performance applications (option 3)

Internal oscillator

The product is equipped with a high stability low phase noise 5 MHz crystal oscillator (BVA-OCXO) for internal frequency generation.

Included Peripheral Equipment

- Hirschmann Stak 20 connector for self cable mounting for connection to the Stakei 2 DC connector at the unit,
- AC supply cord.
- Serial interface cable

Standard CLEAN Module Configuration

Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10
	Oscillator	Option slot	Option slot	Multiplier	PCO	PCO	PCO	PC	DC/DC	AC/DC
	Module			Module	Module	Module	Module	module	Power	Power
	5 MHz			100 MHz	100 MHz					
				1 output >	< 1 input					
	4 outputs			+ 3 outputs	+ 5 inputs				Input	Input
	BNC			SMA	SMA				18-32 V	90-265 V

NOTE: One output of the multiplier module is connected by patch cable to one input of the PCO module (internal reference frequency). The remaining 3 outputs of the multiplier module (100 MHz being derived from the internal oscillator 5 MHz) can be used externally. The remaining 5 inputs of the PCO module can be used for feeding 100 MHz reference signals to the CLEAN. The product delivery comprises the required number of patch cables with a 6 dB attenuator each for making the Multiplier Module output signal compatible to the needs of the PCO Module input needs.

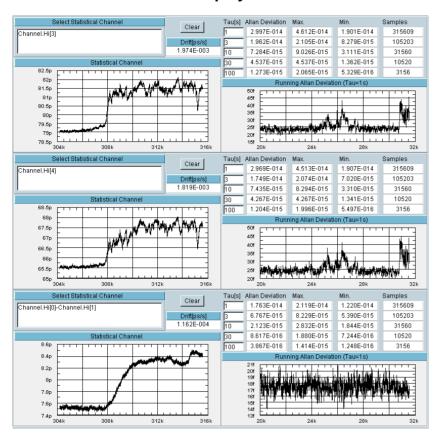
Each of the options 1 to 3 (for the options see "Product Configurations" below) needs an option slot. Up to two options can simultaneously be implemented using the both option slots.

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



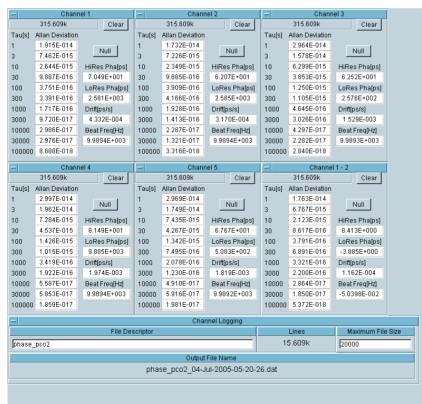
External Visualisation / Display Software



The display software is used to monitor the integrity of the ongoing measurements. It shows the current phase measurement data ("Statistical Channel") and the current ADEV values for tau = 1 sec as a plot over time based on a sliding window analysis of the received measurement data ("Running Allan Deviation"). Furthermore it presents tables of the current ADEV, the minimum ADEV and the maximum ADEV being calculated in the sliding window analysis since start of the measurement for tau = 1 ... 100 sec. In addition, the frequency ('drift') is

This data is continuously provided for each of the five channels.

Any combination of channels (sum, difference) can be selected as a 'virtual channel' as well. For this channel, also ADEV and frequency offset is calculated and displayed.



The following screen shot shows the summary screen of the display software.

It gives the Allan Deviation for tau = 1 to 100 000 sec.

The number given below the headline ("Channel x") gives the number of phase samples being analyzed. Current measurement values are given for both time interval counters, the low resolution one ("LoRes Pha[ps]") and the high resolution one ("HiRes Pha[ps]"). Furthermore the current frequency offset is given ("Drift[ps/s]"). The beat note ("Beat Freq[Hz]") allows the expert checking the integrity of the phase measurement functions.

Also 'virtual channels' can be monitored, here the 6th table gives the difference between channel 1 and channel 2.

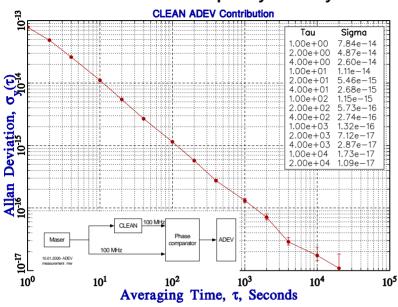
5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



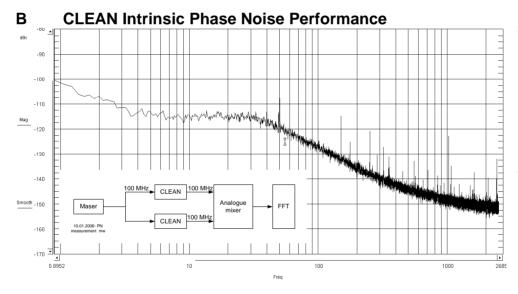
Measurement Results

A CLEAN Intrinsic Frequency Stability Performance



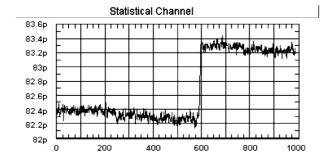
The graph shows the typical ADEV performance of the CLEAN. The measurement had been taken in air conditioned environment with a maximum temperature variation of < 0.5 K_{pp}. The CLEAN Oscillator and an external phase comparator were locked to a common source with a passive splitter.

The time constant of the CLEAN's internal PLL is around 0.6 second by default. It is adjustable in order to allow for optimal filtering of the input signal. Above this time constant, the ADEV drops with a slope of -1 per decade over tau.



The phase noise measurement is made by comparing two 100 MHz outputs of two different CLEANs against each other by means of an analogue mixer and by FFT processing the low frequency output of that mixer. The phase noise performance of a single output is approximately obtained by subtracting 3 dB from this measurement result.

C CLEAN switch-over phase response



In the following measurement one of the input reference signals to the CLEAN Oscillator had been removed while the phase of the CLEAN output signal is recorded versus the phase of the stable measurement reference signal. The resulting phase transient of 1 ps phase step is shown in the screen shot below.

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



Controlling the Clean-up Oscillator

Local Control

The Clean-up Oscillator front panel has a 2 lines 40 characters LCD display and 8 push buttons. This interface allows local control and monitoring of the unit. Especially the IP address of the unit is set via this interface.

Remote Control by Telnet

The Clean-up Oscillator allows for remote control via telnet using its TCP/IP port #23.

TCP Command & Data Output Interface, and Serial Interface

The Clean-up Oscillator supports a management and control interface (M&C) on its TCP/IP ports #2000 and #2001. The same function is also available via a serial RS232 interface. Regularly issued status reports as well as status reports on request are provided. For the data being available for such state reports see the list of monitored parameters below.

UDP Interface

The state reports can be made available also at UDP ports. This allows any external station monitor for getting the CLEAN state just by listening to this port.

Functional upgrades

Firmware upgrade is possible by FTP download.

Configurable Parameters

The following parameters can be configured either via Local Control or via Telnet.

Function	Configurable Parameter	Function	Configurable Parameter
Oscillator and	- Select input reference signal - Enable/disable the control loop	Input	- Set 5 or 10 MHz input (option 2, see below)
control loop	(tracking/holdover) - Control loop time constant - Phase offset - Frequency offset	M&C	Save interval (time interval of regular state reports)Clear system event record
	- Frequency drift (all offsets versus the input reference)	LAN	TCP/IP configurationRemote control enable/disableTelnet connection enable/disable

Monitored Parameters

The Clean-up Oscillator monitors all essential states of its internal hardware as well as the states of the inputs signals, the states of the output signals, the state of the internal oscillator control loop, and the states of the time interval counters.

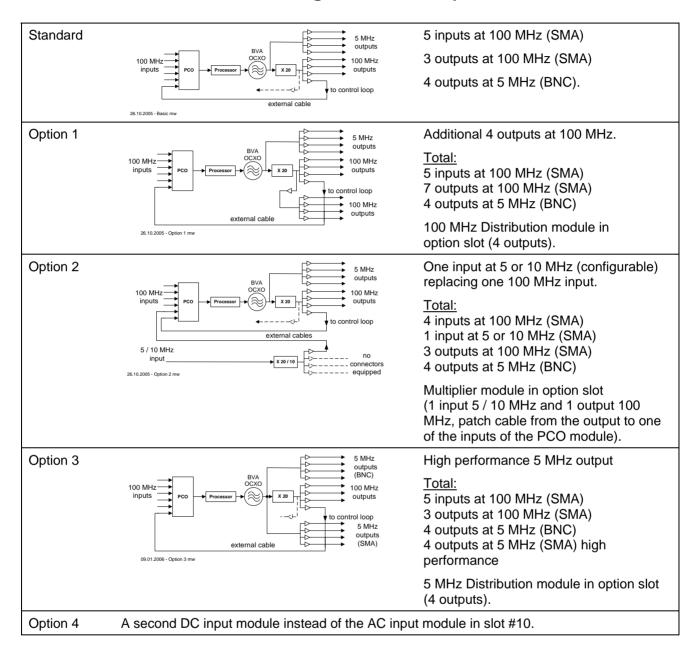
Function	Monitored Parameters	Function	Monitored Parameters
Hardware	- Internal DC voltages	Oscillator	- Control loop offset and status
	Internal currentsUnit internal temperature	PCO	Phase comparator current valuesMeasurement history
Outputs	- Signal power		•

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



Product configurations and options



5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



Internal Oscillator Performance Specification

Stability Perf	ADEV	
Tau	1 sec	1.3 * 10 ⁻¹³
	3 sec	8.0 * 10 ⁻¹⁴
	30 sec	8.0 * 10 ⁻¹⁴

Phase noise @ 5 MHz	dBc/Hz
1 Hz	-125
10 Hz	-145
100 Hz	-153
1 kHz	-156
10 kHz	-156

Aging

Spec 2 * 10⁻¹¹

Typical 1 * 10⁻¹¹

per day after 30 days of continuous operation

Intrinsic Stability and Phase Noise Performance

The following tables give the intrinsic frequency stability and the intrinsic phase noise performance of the CLEAN when using the 100 MHz inputs and outputs.

Tau
1 sec
10 sec
100 sec
1 000 sec ¹⁾
10 000 sec ¹⁾
100 000 sec ¹⁾

ADEV *) 100 MHz				
spec	typ			
1.0 * 10 ⁻¹³	7.9 * 10 ⁻¹⁴			
1.5 * 10 ⁻¹⁴	1.1 * 10 ⁻¹⁴			
1.5 * 10 ⁻¹⁵	1.2 * 10 ⁻¹⁵			
1.5 * 10 ⁻¹⁶	1.3 * 10 ⁻¹⁶			
2.5 * 10 ⁻¹⁷	1.8 * 10 ⁻¹⁷			

Freq. Offset
1 Hz
10 Hz
100 Hz
1 kHz
10 kHz
100 kHz

	dBc/Hz 100 MHz				
	spec	typ			
	-100	-101			
:	-115	-117			
:	-127	-129			
:	-147	-153			
:	-152	-158			
	-153	-159			

Notes

Specification

Measurements

Number of channels Number reference inputs

Virtual channels Real time measurements Measurement output 6

1 (any one of the six channels)
Definition of the reference channel

Any combination of two channels by use of Display Software Phase, frequency, and ADEV per channel

Phase data is collected in files the format of which is compliant to the needs of the STABLE32 software. Storage capacity of an external PC is required for this.

Monitor & Control SW Display SW Display SW Monitor & Control SW

^{*:} ADEV here is the ADEV over the PLL error signal of the clean. In the long run, the CLEAN output is locked to the input signal. In the short run, the CLEAN output removes fluctuations of the input signal. Depending on the quality of the input signal, the loop bandwidth of the digital PLL has to be optimised, which affects the ADEV of the PLL's error signal.

^{1:} Measurements at these time intervals depend heavily on external temperatures. Specified values are guaranteed only in thermally controlled laboratory environment (+18 to +24 $^{\circ}$ C, slopes < 0.2K/h, variation <0.5Kpp). Use of phase stable cables – such as FSJ1, TCOM-400, LMR-400) is mandatory for runs of more than 20 cm. Operation in standard non-climatised environment limits noise floor to some parts in 10^{-17} .

5 / 10 / 100 MHz ultra low phase noise clean-up oscillator Frequency offset and frequency drift compensation

Part No: 10281



100 MHz Input

Impedance 50Ω Connector **SMA**

+0 .. +7 dBm Input Level Frequency 100 MHz, sine wave

< 1 * 10⁻¹² < 5 * 10⁻¹⁰ Frequency offset .. for optimal performance +5 .. +7 dBm .. operational

5 / 10 MHz Input (option)

Impedance Connector **SMA** 50Ω

Input Level +3 .. + 15 dBm Frequency 5 / 10 MHz, sine wave +7 .. + 15 dBm .. for optimal performance Frequency configuration Manual configuration

Frequency offset < 1 * 10-< 5 * 10⁻¹⁰ .. operational

100 MHz Output

Impedance Connector SMA 50 Ω

Output Level $+11.5 \pm 0.5 dBm$ Frequency 100 MHz, sine wave

5 MHz Output (standard performance)

Impedance 50 Ω Connector BNC

Output Level $+12.5 \pm 0.5 dBm$ 5 MHz, sine wave Frequency

5 MHz Output (high performance, option)

Impedance 50 Ω Connector SMA

Output Level $+12.5 \pm 0.5 dBm$ Frequency 5 MHz, sine wave

Electrical interface

Supply voltage DC 18 to 32 V DC With the option 4 the device is equipped with redundant (double) DC input and no AC input.

Supply voltage AC 90 to 265 V AC, 47 to 65 Hz

Source selection Load sharing between AC and DC inputs

Power Consumption < 60 watts

M & C interface

RS232, 9 pin Sub-D male connector Serial line

19200 bps 8N1, plain ASCII Protoco

Availability If not used for time code input or output.

Ethernet 10 Mbit/s twisted pair, RJ45 connector

Service Port Service Port TCP services Telnetd 23 Data output 2001 Command 2000 **UDP** services 514 Data output configurable Syslog client TFTP server 69 NTP client 123

Monitored items ADEV, phase, frequency, PLL lock state, instrument status & control

Commandable items Measurement start, stop, clear Definition of the offset control signal LCD display, 2 lines, 80 characters

Front display Monitor display per channel: signal presence + phase and frequency offset versus the

reference channel.

8 push buttons for basic instrument setup and configuration.

Mechanical

Outline, Weight 19 inch, 2 height units (448.8 mm * 88 mm)

depth 448 mm, weight 8 kg.

Environmental

Transportation and Storage

max 1g acceleration at 8 to 500 Hz

-20°C to +75°C Temperature. 0°C to +40°C Temperature

Humidity 10% to 90% (non condensing) (spec. valid for +18..+24°C, ± 1 K_{pp}, slope < 0.2K/h) < 20 000 m

Operation

Altitude Humidity 20% to 90% (non condensing)

Shock max 10g acceleration for 11 ms Altitude < 3.000 mVibration

max. 0.15 mm at 5 to 8 Hz,

Copyright © 04/2006, TimeTech GmbH Data subject to change without notice. 04 April 2006 Page 11 of 11

TimeTech GmbH Curiestrasse 2 D-70563 Stuttgart Germany

Tel.: ++49 711 67808-0 ++49 711 67808-99 Fax: info@TimeTech.de e-mail: www.TimeTech.de web: